

# CV3 Family

AI Domain Controller for ADAS and L2+ to L4 Autonomy

## Key Features

### Computer Vision AI Engine CVflow®

- Neural network (NN)-based processing to enable detection, classification, tracking, and more
- Neural vector processor (NVP) with industry-leading AI performance per watt
- General vector processor (GVP) for offloading classical computer vision, radar processing, and floating-point intensive algorithms

### Advanced Image Processing

- Multi-exposure, line-interleaved high dynamic range (HDR)
- Real time multi-scale / multi-field of view (FoV) generation
- Hardware dewarping engine support
- Multiple camera support
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor

### Dense Stereo and Optical Flow Engine

- Generic obstacle detection, terrain modeling, and more

### Graphics Processing Unit (GPU)

- Automotive GPU for 3D surround-view rendering

### High-Efficiency Video Encoding

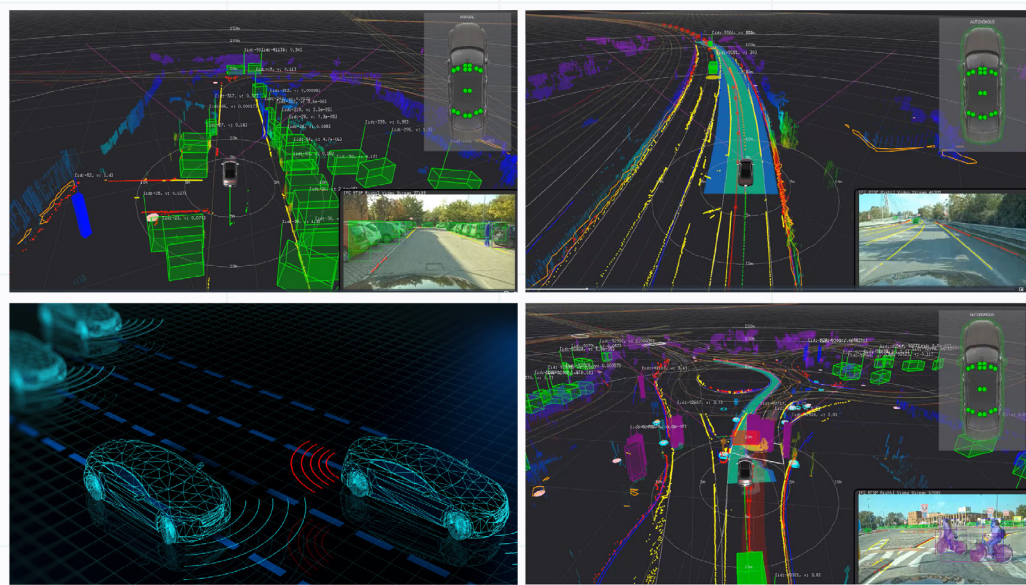
- H.265, H.264, MJPEG video encoding
- Flexible multi-streaming capability

### Functional Safety

- Processing island targeted to meet ASIL B requirements; safety island targeted to meet ASIL D requirements
- Error correcting code (ECC) protection of DRAM
- Central error handling unit (CEHU)

### Target Applications

- Automated driving from L2+ to L4
- Single- / multi-camera advanced driver assistance systems (ADAS)
- Parking assistance systems
- Driver monitoring systems (DMS) and in-cabin solutions
- Single- / multi-channel electronic mirrors with blind spot detection (BSD)

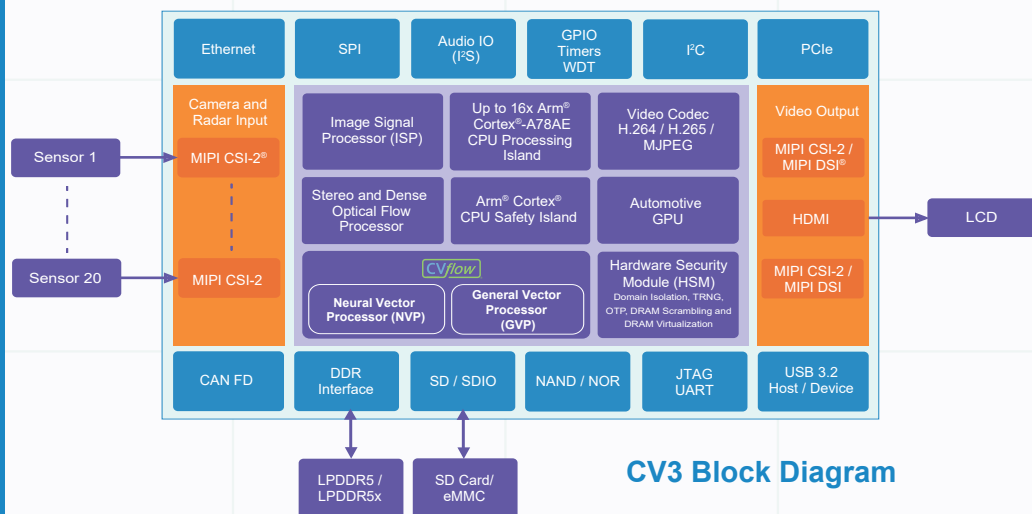


## Overview

Ambarella's ASIL B(D)-compliant CV3 domain controller system on chip (SoC) provides industry-leading AI performance per watt for NN computation, with a performance increase of over 40x compared to Ambarella's prior automotive family of SoCs. In addition, CV3 includes a GVP, an advanced image processor, a dense stereo and optical flow engine, up to 16 Arm® Cortex®-A78AE CPUs, and an automotive GPU, in a single SoC. Ambarella's highly-efficient CVflow®, artificial intelligence (AI) engine enables high performance, low latency, and low-power NN processing for ADAS and L2+ to L4 autonomous vehicles. CVflow's NVP is enhanced to support the latest advancements in NN inference. The NVP is complemented by the new floating-point GVP, designed to offload classical computer vision and radar processing off the NVP engines and floating-point intensive algorithms from the Arm CPUs.

The image signal processor (ISP) provides outstanding imaging in low-light conditions, while its HDR processing extracts maximum image detail in high-contrast scenes, enhancing the AI and computer vision capabilities of the chip while delivering crisp video for viewing. CV3 delivers high-resolution video recording and streaming at very low bit rates with efficient encoding in H.265 and H.264 video formats. It includes a hardware security module (HSM), which provides isolation of different domains, secure software provisioning, a suite of advanced cybersecurity features such as asymmetric / symmetric crypto acceleration, secure storage and key provisioning, encrypted CVflow tasks, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and DRAM virtualization.

Fabricated in an advanced 5 nm process technology, the CV3 is an ideal platform for implementing autonomous driving for vehicles from L2+ to L4, single- and multi-camera ADAS, DMS and in-cabin solutions, single- and multi-channel electronic mirrors with BSD, and intelligent parking assistance systems.



CV3 Block Diagram

# General Specifications

## Computer Vision AI Processor

- CVflow processor optimized for high-performance and power-efficient, neural network compute
- NVP with industry-leading AI performance per watt
- GVP for offloading classical computer vision, radar processing, and floating-point intensive algorithms
- Stereo engine for disparity map generation
- Dense optical flow engine

## Processor Cores

- Up to 16 core Arm® Cortex®-A78AE for processing island
- Arm Cortex lockstep cores for safety island
- NEON™ SIMD and FPU acceleration

## Graphics Processing Unit

- Automotive GPU for 3D surround view rendering

## Camera and Radar Input

- 12x MIPI CSI-2® (4x-lane, MIPI D-PHY)
- Up to 20 cameras using MIPI virtual channels

## Video Output

- HDMI® 2.0 including PHY with consumer electronic control (CEC) support
- Two MIPI CSI-2 / MIPI DSI® ports

## CMOS Sensor / Image Processing

- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)

- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Multi-ROI hardware scaler
- Adjustable auto exposure (AE) / auto white balance (AWB)
- Dynamic range (WDR and HDR) engine
- Chromatic aberration correction
- Geometric distortion correction
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

## Video Encoding

- H.264 / H.265 MP / HP L5.0 and MJPEG
- Flexible group of pictures (GOP) configuration with I and P frames
- Multiple CBR and VBR rate control modules

## Hardware Security Module (HSM)

- Asymmetric / symmetric crypto acceleration, domain isolation, secure storage and key provisioning, encrypted CVflow tasks, TRNG, OTP, DRAM scrambling, and DRAM virtualization

## Tools for Development

- Neural network toolkit to ease the porting of NNs trained using frameworks such as Caffe, TVM, PyTorch, TensorFlow, TensorFlowLite, Keras, and ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

## Memory Interfaces

- LPDDR5 / LPDDR5x, up to 256-bit data bus for data, up to 128 GB capacity
- Multiple SD controllers
- Boot from PCIe / SPI NAND / SPI NOR / USB / eMMC
- Single- / dual- / quad- / octal-SPI NOR and single- / dual- / quad-SPI NAND

## Peripheral Interfaces

- Multiple 10 / 100 / 1000 Ethernet with RMII / RGMII
- Multiple 4-lane PCIe interfaces
- USB 3.2 host / device and USB 2.0 device only with PHY
- I<sup>2</sup>S input and output interfaces, DMIC
- Multiple CAN FD interfaces
- Multiplexed UART and I/F of SSI / IDC
- Multiple GPIO ports, PWM, and IR interfaces
- Watchdog timer, general purpose timers, and JTAG

## Physical

- 5 nm low-power complimentary metal-oxide semiconductor (CMOS)
- HFC BGA package
- Operating temperature -40°C to +125°C (T<sub>J</sub>)
- Automotive qualified (AEC-Q100 Grade-2, ASIL B(D))

# CV3 Domain Controller Development Platform

The CV3 domain controller development platform contains the necessary tools, software, hardware, and documentation to develop ADAS and L2+ to L4 autonomous vehicles utilizing the powerful CVflow processor, while supporting development of customized features.

## Evaluation Kit (EVK)

- CV3 main board with connectors for sensor / lens board and peripherals
- Sensor boards
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code available with additional licensing

## Software Development Kit (SDK)

- SDK, OS, and middleware
- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation with programmer's guide and more
- Tools to optimize, port, and profile NN / DNN

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