Ambarella
AI envisioned

PRODUCT BRIEF

CV3-AD685

AI Central Domain Controller for ADAS and L2+ to L4 Autonomy

Key Features

AI Engine CVflow®
- Neural vector processor (NVP) with industry-leading AI performance per watt and neural network (NN)-based processing to enable detection, classification, tracking, and more
- General vector processor (GVP) for offloading classical computer vision and radar processing

Advanced Image Processing
- Multi-exposure, line-interleaved high dynamic range (HDR)
- Real time multi-scale / multi-field of view (FoV) generation
- Hardware dewarping engine support

Stereo and Dense Optical Flow Engine
- Generic obstacle detection, terrain modeling, ego motion, and more

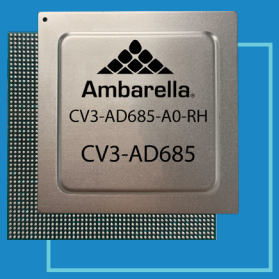
Central Processing Unit (CPU)
- Arm® Cortex®-A78AE and Cortex-R52 CPUs

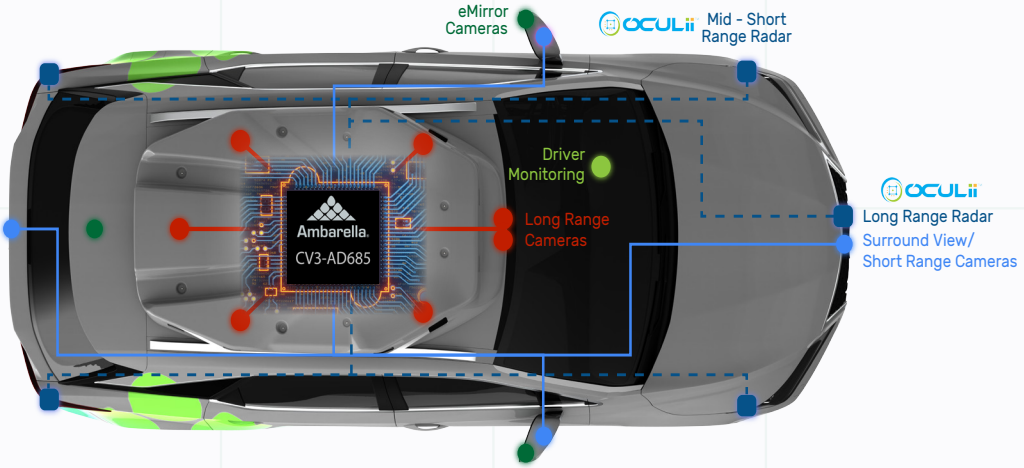
Graphics Processing Unit (GPU)
- Automotive GPU for 3D surround-view rendering

High-Efficiency Video Encoding
- H.265, H.264, and MJPEG video encoding

Functional Safety
- Processing island targeted to meet ASIL B requirements; safety island targeted to meet ASIL D requirements
- Error correcting code (ECC) protection of DRAM
- Central error handling unit (CEHU)

Target Applications
- Assisted and automated driving for L2+ to L4
- Multi-sensor ADAS
- Parking assistance and automated parking systems
- Driver monitoring systems (DMS) and in-cabin solutions
- Multi-channel electronic mirrors with blind spot detection (BSD)



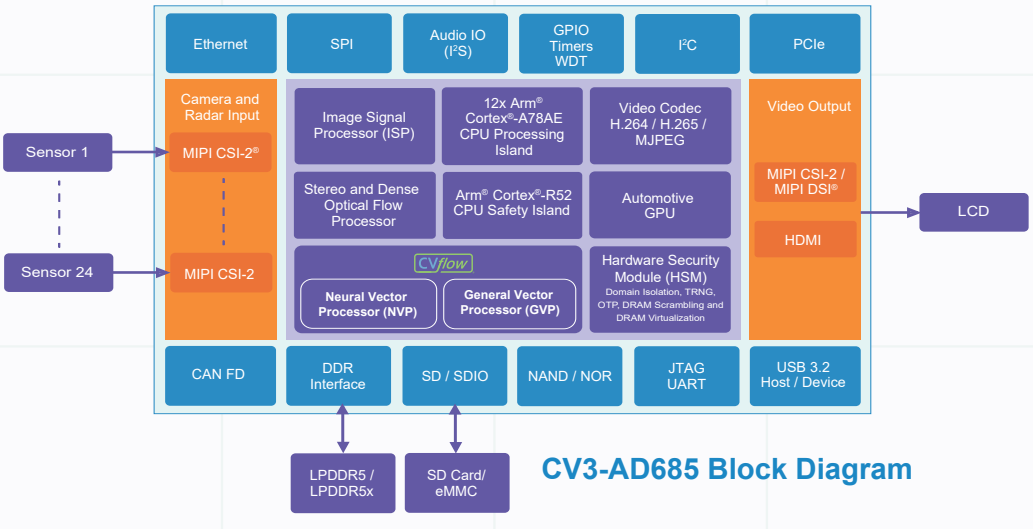


Overview

Ambarella's ASIL B(D)-compliant CV3-AD685 artificial intelligence (AI) domain controller system on chip (SoC) supports multi-sensor perception, fusion and path planning for L2+ to L4 autonomous driving, and premium advanced driver assistance systems (ADAS) products. CV3-AD685 includes Ambarella's highly-efficient CVflow® AI engine (NVP / GVP) to enable high performance, low latency, and low-power NN processing. CVflow's NVP is enhanced to support the latest advancements in NN inference including support for transformer networks, while the GVP provides the acceleration for traditional computer vision and radar processing. In addition, CV3-AD685 includes an advanced image signal processor (ISP), a dense stereo and optical flow engine, up to 12 Arm® Cortex®-A78AE CPUs, 3 pairs of Arm Cortex-R52 lockstep cores for the safety island, an automotive GPU, and a hardware security module (HSM), all in a single SoC. The CV3-AD685 SoC is designed to support cameras, radars, lidars, and ultrasonic sensors. CV3-AD685's "algorithm first" architecture supports the entire AD software stack.

The image signal processor (ISP) provides outstanding imaging in low-light conditions, while its HDR processing extracts maximum image detail in high-contrast scenes, enhancing the AI and computer vision capabilities of the chip and delivers crisp video for viewing. CV3-AD685 delivers high-resolution video recording and streaming at very low bit rates with efficient encoding in H.265 and H.264 video formats. It includes a hardware security module (HSM), which provides isolation of different domains, secure software provisioning, a suite of advanced cybersecurity features such as asymmetric / symmetric crypto acceleration, secure storage and key provisioning, encrypted CVflow tasks, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and DRAM virtualization.

Fabricated in an advanced 5 nm process technology, the low power consumption CV3-AD685 SoC is an ideal platform for efficiently implementing assisted and autonomous driving for L2+ to L4 vehicles, multi-sensor ADAS, DMS and in-cabin solutions, multi-channel electronic mirrors with BSD, and intelligent parking assistance and automated parking systems.



CV3-AD685 Block Diagram

General Specifications

Computer Vision AI Processors
- CVflow processor provides high-performance and power-efficient neural network computing
- NVP with industry-leading AI performance per watt
- GVP for accelerating classical computer vision and radar processing
- Stereo engine for disparity map generation and dense optical flow engine

Processor Cores
- 12 core Arm® Cortex®-A78AE for the processing island
- 3 pairs of Arm Cortex-R52 lockstep cores for the safety island
- NEON™ SIMD and FPU acceleration

Graphics Processing Unit
- Automotive GPU for 3D surround view rendering

Camera and Radar Input
- 8x MIPI C-PHY / D-PHY for camera and radar inputs
- Up to 24 cameras using MIPI virtual channels

Video Output
- HDMI® 2.0 including PHY with consumer electronic control (CEC) support
- 2 MIPI CSI-2 / MIPI DSI® ports

CMOS Sensor / Image Processing
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)
- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Multi-ROI hardware scaler
- Adjustable auto exposure (AE) / auto white balance (AWB)
- Dynamic range (WDR and HDR) engine
- Chromatic aberration correction
- Geometric distortion correction
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

Video Encoding
- H.264 (MP / HP) / H.265 (MP) and MJPEG
- Flexible group of pictures (GOP) configuration with I and P frames
- Multiple CBR and VBR rate control modules
- Flexible multi-streaming capability

Hardware Security Module (HSM)
- Asymmetric / symmetric crypto acceleration, domain isolation, secure storage and key provisioning, encrypted CVflow tasks, TRNG, OTP, DRAM scrambling and virtualization

Tools for Development
- Neural network toolkit to ease the porting of NNs trained using frameworks such as Caffe, TVM, PyTorch, TensorFlow, TensorFlowLite, Keras, and ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

Memory Interfaces
- LPDDR5 / LPDDR5x, up to 256-bit data bus for data, up to 128 GB capacity
- Multiple SD controllers
- Boot from PCIe / SPI NAND / SPI NOR / USB / eMMC
- Single- / dual- / quad- / octal-SPI NOR and single- / dual- / quad-SPI NAND

Peripheral Interfaces
- Multiple 10 / 100 / 1000 Ethernet with RMII / RGMII
- Multiple PCIe interfaces
- USB 3.2 host / device and USB 2.0 device only with PHY
- I²S input and output interfaces, DMIC
- Multiple CAN FD interfaces
- Multiplexed UART and I/F of SSI / IDC
- Multiple GPIO ports, PWM, and IR interfaces
- Watchdog timer, general purpose timers, and JTAG

Physical
- 5 nm low-power complimentary metal-oxide semiconductor (CMOS)
- HFC BGA package
- Operating temperature -40°C to +125°C (T_J)
- Automotive qualified (AEC-Q100 Grade-2, ASIL B(D))

CV3-AD685 Domain Controller Development Platform

The CV3-AD685 domain controller development platform contains the necessary tools, software, hardware, and documentation to develop ADAS and L2+ to L4 autonomous vehicles utilizing the powerful CVflow processor, while also supporting development of customized features.

Evaluation Kit (EVK)
- CV3-AD685 main board with connectors for sensor / lens and peripherals
- Camera modules
- Datasheet, BOM, schematics, and layout
- SDK and reference application with source code available with additional licensing

Software Development Kit (SDK)
- SDK, OS, and middleware
- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation with programmer's guide and more
- Tools to optimize, port, and profile NN / DNN

www.ambarella.com/contact-us/

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