Ambarella
AI envisioned™

S5L

IP Camera SoC

Key Features

Flexible Low-Power Platform
- 64-bit quad-core Arm® Cortex®-A53 CPU up to 1.0 GHz with L2 cache
- Linux kernel version 4.9 or later (64-bit)
- Linux software development kit (SDK) for standards-based development

Advanced Image Processing
- Up to 480 Mpixel/s input rate
- Multi-exposure line-interleaved high dynamic range (HDR)
- Hardware lens distortion correction (LDC)
- Electronic image stabilization (EIS)
- Dual independent sensor inputs
- 3D motion-compensated noise reduction (MCTF)

High-Efficiency Video Encoding
- H.264 and H.265 video compression
- Flexible multi-streaming
- Up to 4KP30 + 480p30 video performance for H.265
- Smart H.264 and H.265 encoder algorithms

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Overview

The Ambarella S5L IP camera system on chip (SoC) integrates an advanced image signal processor (ISP), H.265 and H.264 encoders capable of up to 4KP30 video, and a quad-core Arm® Cortex®-A53 CPU up to 1 GHz for implementing custom applications. The low-power S5L is suitable for a wide range of Internet protocol (IP) camera designs, offering advanced imaging features such as high dynamic range (HDR) processing, motion-compensated 3D noise reduction, dual video input (VIN), and lens distortion correction (LDC).

The flexible S5L software development kit (SDK) provides a Linux-based framework and development environment that includes image-tuning tools and a rich set of application programming interfaces (APIs), enabling a range of product customization and differentiation options in areas such as sensor and lens tuning, analytics, and network applications.
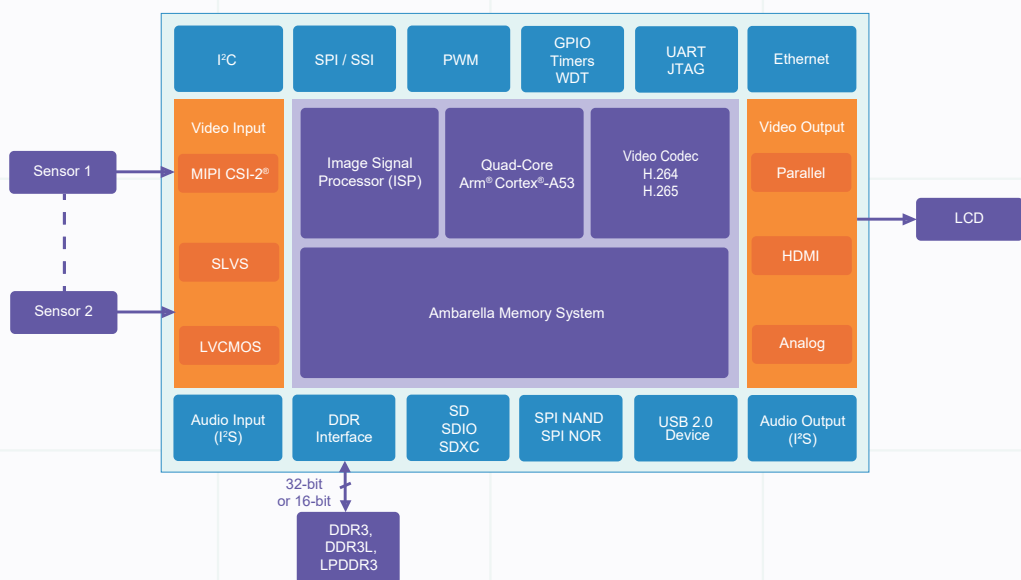
S5L Block Diagram
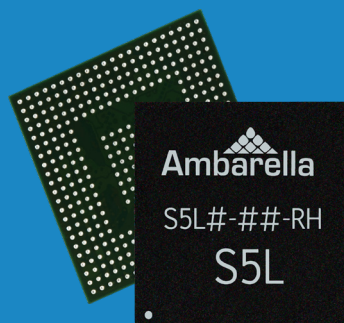
General Specifications

Processor Cores
- Quad-core Arm® Cortex®-A53 up to 1.0 GHz
- 32 KB / 32 KB I/D and 256 KB L2 cache
- NEON™ and FPU acceleration
- AES / 3DES / SHA-1 / MD5 cryptography engine
- Ambarella image and video digital signal processors (DSPs)

Sensor and Video I/O
- Single or dual sensor input (LVDS / MIPI®) with independent ISP configuration
  - Single 8-lane sub-LVDS / SLVS / HiSPi™ or dual 4-lane MIPI
  - 14-bit parallel and LVCMOS sensors
- BT.601 / 656 / 1120 video in and BT.656 / BT.1120 out
- 24-bit RGB out, HDMI® 1.4b with PHY out
- PAL / NTSC composite SD video out

Front End Sensor Processing
- 480 MHz maximum pixel rate
- Lens shading
- Multi-exposure high dynamic range (HDR) (line-interleaved sensors)
- Wide dynamic range (WDR) local exposure

Image Processing
- 3D motion-compensated noise reduction (MCTF)
- 3-axis electronic image stabilization (EIS)
- Adjustable auto exposure (AE) / auto white balance (AWB) / auto focus (AF)

- 180° fisheye lens distortion correction (LDC)
- High-quality polyphase scalers
- Digital pan / tilt / zoom (DPTZ) and virtual cameras
- On-screen display (OSD) engine, overlays, and privacy mask
- Crop, mirror, flip, and 90° / 270° rotation
- DC-iris and P-iris
- Defect pixel correction
- Geometric and chroma lens distortion correction
- Gamma compensation and color enhancement
- Backlight compensation

Intelligent Video Analytics
- Advanced third-party analytics options:
  - Face detection and tracking
  - Intelligent motion detection
  - Tampering / intrusion detection and people counting
  - License plate recognition
  - Object recognition and more

Video Encoding
- H.265 (HEVC) MP L5.1, H.264 BP / MP / HP L5.1 and MJPEG
- 4KP30 + 480p30 maximum encoding performance
- Up to 8 simultaneous stream encodes
- SmartAVC and SmartHEVC low bit rate streaming
- Flexible group of pictures (GOP) configuration with I, P, and B frames

- Temporal scalable video codec with four layers (SVC-T)
- Dynamic region of interest (ROI) with 32 free-form regions
- Multiple CBR and VBR control modes

Memory Interfaces
- DDR3 / DDR3L / LPDDR3 up to 1 GHz and 32-bit or 16-bit data bus
- Two SD controllers with SDXC SD™ card
- NAND flash and SLC with ECC
- Boot from SPI-NOR, SPI-EEPROM, NAND flash, USB, or eMMC

Peripheral Interfaces
- 10 / 100 / 1000 Ethernet with RMII / RGMII
- Two USB ports: one for host and one for host / device
- Multiple I²S, SSI / SPI, I²C, and UART
- Many GPIO ports, PWM, steppers, IR, and ADC
- Watchdog timer, multiple general purpose timers, and JTAG

Physical
- 14 nm low-power complimentary metal-oxide semiconductor (CMOS)
- Operating temperature -20°C to +85°C
- FC LFBGA package with 369 balls, 14x14 mm, 0.65 mm pitch rate

S5L IP Camera Development Platform

The S5L camera development platform contains the necessary tools, software, hardware, and documentation to develop an IP camera while supporting development of customized features.

Evaluation Kit (EVK)

- S5L main board with connectors for sensor / lens board and peripherals
- Sensor board: OmniVision, onsemi, Panasonic, Sony, and others
- Datasheet, BOM, schematics, and layout
- IP camera reference application with C and C++ source code available with additional licensing

Software Development Kit (SDK)

- Linux 4.9 or later with 64-bit kernel including patches, drivers, tools, and application source code
- Latest Linaro GCC Toolchain for 64-bit Arm Cortex ArmV8
- Royalty-free libraries for ISP, 3A, dewarp, and codecs
- Image tuning and manufacturing calibration tools
- Detailed documentation, including a programmer's guide and more

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