

H22A

Video SoC for Dashcam

Key Features

Flexible Low-Power Platform

- Quad-core Arm® Cortex®-A53 CPU up to 1 GHz
- Multiple OS support: ThreadX, Linux, ThreadX + Linux
- 14-nm low-power CMOS process

Advanced Image Processing

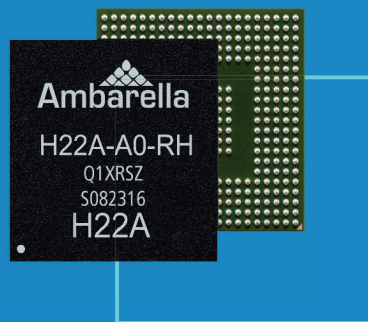
- Multi-sensor support
- Multi-exposure line-interleaved HDR
- Hardware dewarping engine
- Electronic image stabilization (EIS)
- 3D motion-compensated noise reduction (MCTF)
- Superior low-light processing

High-Efficiency Video Codec

- 12MP30 H.264 / H.265 video compression
- Flexible multi-stream capability
- JPEG encoder for stills
- Constant bit rate (CBR) and variable bit rate (VBR) control modes

Target Applications

- Multi-channel drive recorders
- Driver monitoring systems (driver distraction / driver drowsiness detection)

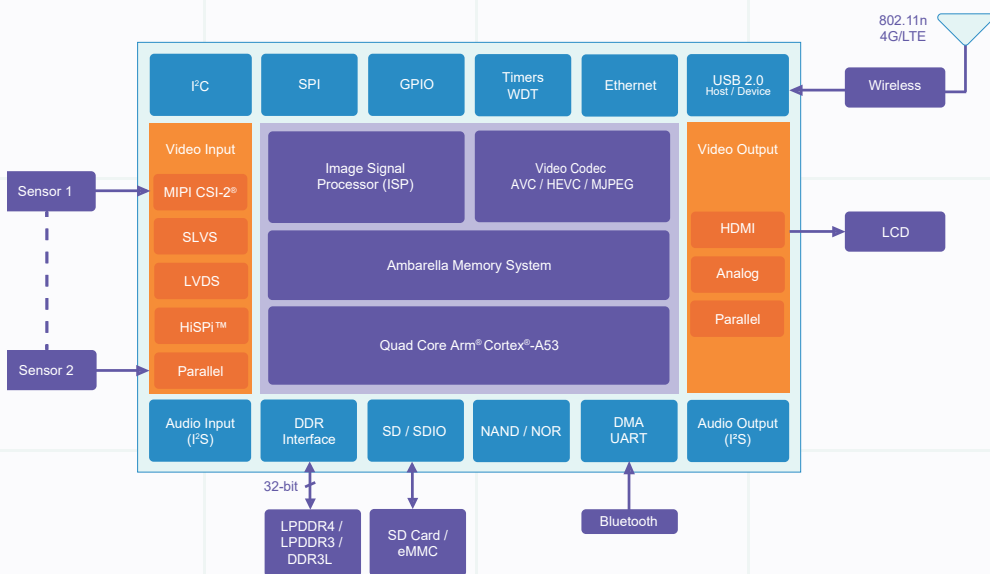


Overview

Ambarella's H22A SoC combines image / video processing and 12MP30 video encoding / decoding in a single low-power design, making it an ideal choice to power the next generation of automotive dash cameras and video recorders. Fabricated in a 14-nm process technology, the chip achieves an industry-leading combination of low power and high performance in both human vision and advanced driver assistance system (ADAS) applications.

H22A implements a highly-efficient 12MP30 AVC (H.264) / HEVC (H.265) encoder / decoder in hardware, along with an industry-leading image signal processor (ISP). H22A's ISP provides outstanding imaging in low-light conditions while high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes. The flexible architecture allows encoding of multiple streams that are optimized for storage and simultaneous video streaming over WiFi and BLE. The chip also supports cameras with ultra-wide-angle lenses by performing highly-efficient distortion correction.

H22A's multi-sensor input enables recording systems that require two or more independent sensor inputs. The quad-core Arm® Cortex®-A53 cores allow implementation of ADAS features such as forward collision warning, lane departure warning, driver monitoring, license plate detection and recognition, and more. To help customers implement their applications, Ambarella provides a software development kit (SDK) available in RTOS (ThreadX) / Linux / RTOS + Linux (dual OS).



H22A Block Diagram

General Specifications

Processor Cores

- Quad-core Arm® Cortex®-A53 up to 1 GHz
- 32 KB / 32 KB I/D and 256 KB L2 cache
- NEON™ SIMD acceleration
- Ambarella image signal processor (ISP)
- AVC / HEVC video codec

Video Input

- Single- or dual-sensor inputs with independent ISP configuration
- MIPI CSI-2® / LVDS / SLVS / HiSPi™
- 14-bit parallel LVCMOS (BT. 601 / 656)

Video Output

- HDMI® 2.0 with PHY out
- PAL / NTSC composite SD video out
- 16-bit parallel LVCMOS (BT. 601)

Memory Interfaces

- LPDDR4 (H22N) and LPDDR3 / DDR3 / DDR3L (H22), up to 1 GHz clock rate, 32-bit data bus, and up to 2 GB capacity
- Two SD controllers: SD0 and SD1
- Boot from SPI NOR / NAND flash / USB / eMMC

Peripheral Interfaces

- One USB 2.0 port configurable as host / device
- 10 / 100 / 1000 Ethernet with RMI / RGMII
- Audio interface including I²S and DMIC
- Multiple SSI / SPI, I²C / IDC, and UART
- Multiple GPIO ports, PWM, IR, and ADC
- Watchdog timer, multiple general purpose timers, and JTAG

CMOS Sensor Processing / Image Processing

- RGGB and monochrome sensor support
- Multi-exposure HDR (line-interleaved sensors)
- Dynamic range (WDR and HDR) engine
- 3D motion-compensated temporal filtering (MCTF)
- Adjustable AE and AWB
- 3-axis electronic image stabilization (EIS)
- Lens distortion correction (LDC) for wide-angle lens
- Crop, mirror, flip, and 90° / 270° rotation
- Defect pixel correction
- Chromatic aberration compensation
- Gamma compensation and color enhancement
- Black level correction
- Lens shading correction

Video Encoding / Decoding

- H.265 MP L5.1, H.264 MP / HP L5.1, and MJPEG
- 12MP30 (360 MPixel/s) maximum encoding performance
- Up to 8 simultaneous stream encodes
- Flexible GOP configuration with I, P, and B frames
- Temporal scalable video codec (SVC-T) with 4 layers
- Dynamic region of interest (ROI)
- Multiple CBR and VBR control modes

Physical

- 14 nm low-power CMOS
- FC LFBGA package (369 balls, 14x14 mm, 0.65 mm pitch) or FC TFBGA (369 balls, 11x11 mm, 0.5 mm pitch)
- Operating temperature -20°C to +85°C (additional operational temperature options available)

H22A Camera Development Platform

The H22A camera development platform contains the necessary tools, software, hardware, and documentation to develop a small form factor camera.

Evaluation Kit (EVK)

- H22A main board with connectors for sensor / lens board and peripherals
- Sensor board: OmniVision, Onsemi, Sony, and others
- Datasheet, BOM, schematics, and layout
- Reference application with C source code available with additional licensing

Software Development Kit (SDK)

- ThreadX / Linux / ThreadX + Linux with patches, drivers, tools, and application source code
- Royalty-free libraries for ISP, 3A, dewarp, and codecs
- Image tuning and manufacturing calibration tools
- Detailed documentation, including a programmer's guide and more

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