

CV5S

8K AI Vision Processor

Key Features

Flexible Low-Power Platform

- CVflow® computer vision engine
- 64-bit dual-core Arm® Cortex®-A76 CPU up to 1.6 GHz
- Linux kernel version 5.10 or later (64-bit)

High-Efficiency Video Encoding

- H.265 and H.264 video compression
- Flexible multi-streaming capability
- 8KP30 video performance
- Multiple constant bit rate (CBR) and variable bit rate (VBR) control modes
- Smart H.264 and H.265 encoder algorithms

Computer Vision Engine

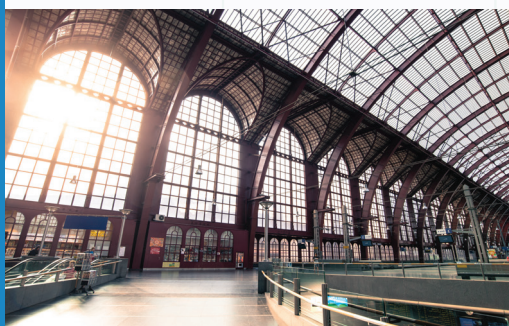
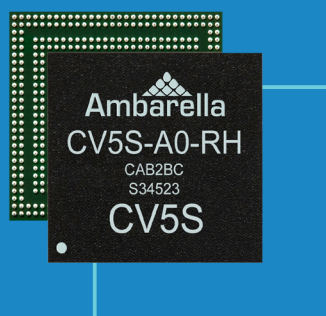
- Convolutional neural network (CNN) / deep neural network (DNN)-based processing: detection, classification, and more
- Accelerators for conventional computer vision (CV) operations
- CNN toolkit for easy porting of neural networks implemented in Caffe, TensorFlow, PyTorch, or ONNX frameworks

Advanced Image Processing

- Multi-exposure line-interleaved HDR
- Hardware dewarping engine
- Electronic image stabilization (EIS)
- Multiple camera support
- 3D motion-compensated temporal filtering (MCTF)
- Superior low-light processing
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support

Target Applications

- Professional internet protocol (IP) cameras
- Intelligent traffic system (ITS) cameras
- Machine vision and robotics applications



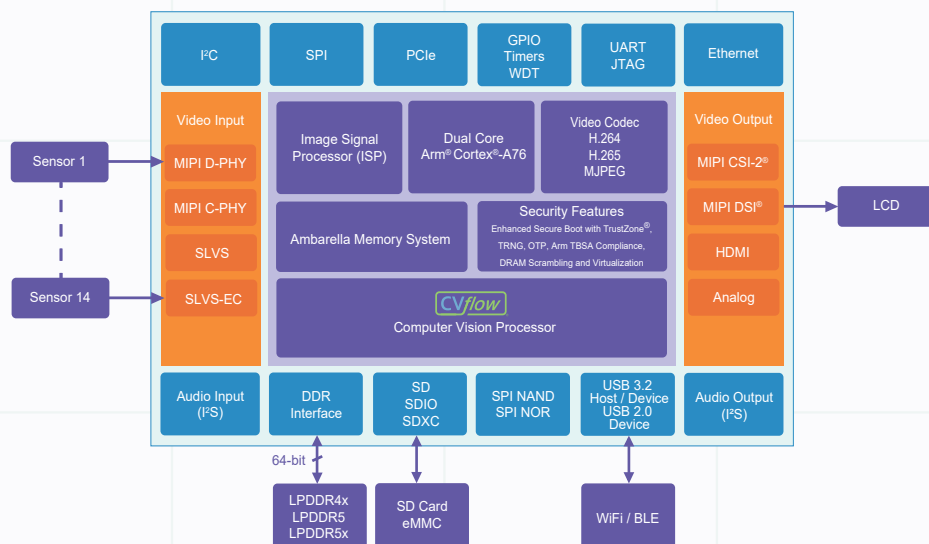
Overview

Ambarella's CV5S system on chip (SoC) provides 8K image processing, video encoding / decoding, and CVflow® computer vision processing in a single, low-power design. Fabricated in advanced 5 nm process technology, CV5S achieves power consumption below 4W for 8K video recording at 30 fps. CV5S's CVflow architecture provides DNN multi-processing required for the next generation of intelligent cameras.

CV5S's advanced image signal processor (ISP) provides outstanding imaging in low-light conditions, while high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, further enhancing the computer vision capabilities of the chip. CV5S includes efficient 8K encoding in both AVC and HEVC video formats, delivering high-resolution video recording and streaming with very low bit rates.

The CV5S's CVflow architecture enables computer vision processing at full 8K, enabling image recognition over long distances and with high accuracy. The CVflow engine can efficiently run multiple neural networks (NNs) in parallel while accelerating classical computer vision algorithms, providing powerful computer vision acceleration at minimal power consumption. To help customers easily port their own neural networks onto the CV5S SoC, Ambarella's software development kit (SDK) offers a complete set of tools for software and artificial intelligence (AI) implementation.

CV5S includes a suite of advanced security features to implement on-device physical security, including enhanced secure boot with TrustZone® and secure memory, true random number generator (TRNG), one-time programmable memory (OTP), Arm® trusted base system architecture (TBSA) compliance, DRAM scrambling, and virtualization.



CV5S Block Diagram

General Specifications

Processor Cores

- Dual-core Arm® Cortex®-A76 up to 1.6 GHz
- 64 KB / 64 KB L1 cache and 256 KB L2 cache per Cortex-A76
- 1024 KB L3 cache per dual-core Cortex-A76
- NEON™ SIMD and FPU acceleration
- AES / SHA-2 / ED25519 crypto acceleration

Computer Vision Processor

- CVflow processor with parallel architecture to boost performance of the low-level portion of perception algorithms

Video Input

- 12-lane SLVS-EC (1–8 lane single link, 1–6 lane * 2 dual link)
- 2x MIPI DC-PHY®
 - Each DC-PHY supports C-PHY mode (1–3 lanes) or D-PHY mode (1–4 lanes)
- 2x MIPI D-PHY (1–4 lanes each)
- 2x SLVS (1–4 lanes each)
- Up to 14 cameras using MIPI virtual channels

Video Output

- HDMI® 2.0 including PHY with consumer electronic control (CEC) support
- PAL / NTSC composite SD video
- 2x MIPI DSI / CSI-2

CMOS Sensor / Image Processing

- Processing up to 8KP30
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)

- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Adjustable AE / AWB / AF
- Advanced dynamic range (WDR and HDR) engine
- Chromatic aberration correction
- 180° and 360° fisheye lens and geometric distortion correction
- On-screen display (OSD) engine and overlays
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, and 90° / 270° rotation

Video Encoding / Decoding

- H.265 (HEVC) MP L6.1, H.264 (AVC) MP / HP L6.1, and MJPEG
- 8KP30 maximum encoding / decoding performance
- Flexible group of pictures (GOP) configuration with I, P, and B frames
- Multiple CBR and VBR rate control modules

Security Features

- Enhanced secure boot with TrustZone® and secure memory, TRNG, OTP, Arm TBSA compliance, DRAM scrambling, and virtualization

Tools for Development

- CNN toolkit to ease the porting of CNNs trained using frameworks such as Caffe, PyTorch, TensorFlow, or ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

Memory Interfaces

- LPDDR4x up to 3.6 Gbits/s/pin, 64-bit data bus, up to 16 GB capacity for LPDDR4x
- LPDDR5(x) up to 5.6 Gbits/s/pin, 64-bit data bus, up to 32 GB capacity for LPDDR5(x)
- Three SD controllers
- Single- / dual- / quad- / octal-SPI NOR and single- / dual- / quad-SPI NAND
- Boot from SPI NAND / SPI NOR / USB / eMMC

Peripheral Interfaces

- 10 / 100 / 1000 Ethernet with RMII / RGMII
- 4-lane PCIe
- 1x USB 3.2 host / device and 1x USB 2.0 device only with PHY
- 2x I²S input and output interfaces, 1x DMIC
- 2x CAN FD interface
- Multiplexed 5x UART and 6 I/F of SSI / IDC
- Multiple GPIO ports, PWM, IR, and ADC
- Watchdog timer, general purpose timers, and JTAG

Physical

- 5 nm low-power complimentary metal-oxide semiconductor (CMOS) technology
- 16 mm x 16 mm FC TFBGA with 0.5 mm ball pitch
- Operating temperature -25°C to +85°C

CV5S Camera Development Platform

The CV5S camera development platform contains the necessary tools, software, hardware, and documentation to develop a camera utilizing the powerful CVflow processor while supporting the development of customized features.

Evaluation Kit

- CV5S main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, onsemi, Omnivision, and others
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code available with additional licensing

Software Development Kit

- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation, including a programmer's guide and more
- CNN / DNN model preparation, porting, and profiling tools

www.ambarella.com/contact-us/

Copyright Ambarella International LP. All rights reserved. Ambarella and the Ambarella logo are trademarks of Ambarella International LP. All other brands, product names, and company names are trademarks of their respective owners. The information in this document is believed to be reliable, but may project preliminary functionality not yet available. Ambarella makes no guarantee or warranty concerning the accuracy and availability of said information and shall not be responsible for any loss or damage whatever nature resulting from the use of, or reliance upon it. Ambarella does not guarantee that the use of any information contained herein will not infringe upon patent, trademark, copyright, or other rights of third parties. Ambarella reserves the right to make changes in the product and / or its specifications presented in this publication at any time without notice.