Ambarella’s ASIL C-compliant CV2FS combines high-performance and power-efficient computer vision acceleration, superior image processing (ISP), and H.264 video compression in a single SoC. Ambarella’s highly efficient CVflow® computer vision engine delivers deep neural network (DNN) processing and a dedicated stereo vision accelerator to enable efficient implementation of mono and stereo algorithms for the next generation of intelligent automotive cameras.

The ISP provides outstanding imaging in low-light conditions while its high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, enhancing the computer vision capabilities of the chip while delivering crisp video for driver viewing. CV2FS delivers high-resolution video recording and streaming at very low bit rates with efficient encoding in H.264 video format. It includes a suite of advanced cybersecurity features such as secure boot with TrustZone®, secure memory, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and virtualization, and a programmable secure level for each peripheral interface.

Fabricated in advanced 10 nm process technology, the CV2FS achieves an industry-leading combination of high performance and low power for computer vision applications. It is an ideal platform for implementing single- and multi-camera advanced driver assistance systems (ADAS), driver monitoring systems (DMS) and in-cabin solutions, single- and multi-channel electronic mirrors with blind spot detection (BSD), and intelligent parking assistance systems.
CV2FS Camera Development Platform

The CV2FS camera development platform contains the necessary tools, software, hardware, and documentation to develop a camera utilizing the powerful CVflow processor while supporting development of customized features.

**Evaluation Kit (EVK)**
- CV2FS main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, ON Semi, Omnivision, and others
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code

**Software Development Kit (SDK)**
- ISO 26262-compliant SDK, OS, and middleware
- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Safety documentation for applications required to meet ISO 26262 standards
- Detailed documentation with programmer’s guide and application notes
- CNN / DNN training, profiling, and porting tools

**General Specifications**

**Processor Cores**
- Quad-core Arm® Cortex®-A53 up to 1 GHz
  - 32 KB / 32 KB L1 cache, 1 MB L2 cache
- Arm Cortex-R52 456 MHz with DCLS (dual-core lock step)
  - 32 KB / 32 KB I/D L1 cache, 1 MB of embedded SRAMs
- NEON™ SIMD and FPU acceleration
- AES / SHA1 / SHA2-256 crypto acceleration using Arm V8 extensions

**Computer Vision Processor**
- CVflow processor optimized for high-performance CNN / DNN execution
- Disparity mapping
- Dense optical flow engine

**Video Input**
- Multi-sensor input with independent ISP configuration
- Three MIPI CSI-2® ports (one port with virtual channels)

**Video Output**
- Two MIPI CSI-2 / MIPI DSI® ports
- OSD engine and overlays

**CMOS Sensor / Image Processing**
- Processing up to 480 MPixel/s
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)

**Video Encoding**
- H.264 MP / HP L5.0
- 8MP30 maximum encoding performance
- Flexible GOP configuration with I and P frames
- Multiple CBR and VBR rate control modules

**Security Features**
- Secure boot with TrustZone®, TRNG, OTP, DRAM scrambling and virtualization

**Tools for Development**
- CNN toolkit to ease the porting of CNNs trained using frameworks such as Caffe, TensorFlow, or ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

**Memory Interfaces**
- LPDDR4x / LPDDR4 up to 1.8 GHz clock rate, 32-bit data bus for data and 16-bit data bus for ECC, up to 4 GB capacity
- Two SD controllers
- Boot from SPI / SPI NAND with BCH / SPI NOR / USB / eMMC

**Peripheral Interfaces**
- Six CAN FD controllers
- Two Ethernet ports with data transfer rates of 10- / 110- / 1000-Mbps
- One USB 2.0 port configurable as device / host with PHY
- Multiple SPI / I2C, IIC, and UART
- Multiple GPIO ports, PWM, steppers, ADC
- Watchdog timer, general purpose timers, and JTAG
- Audio interface (I²S)

**Physical**
- 10 nm low power CMOS
- FC TFBGA package (14x14 mm, 0.65 mm pitch)
- Operating temperature -40°C to +125°C (T_J)
- Automotive qualified (AEC-Q100 Grade-2, ASIL C)