

CV2FS

Automotive Computer Vision SoC

Key Features

Computer Vision Engine CVflow®

- Convolutional neural network (CNN)- / deep neural network (DNN)-based processing to enable detection, classification, tracking, and more
- Dense optical flow engine
- Tools for high- and low-level algorithm development
- CNN toolkit for easy porting with Caffe, PyTorch, TensorFlow, and ONNX

Stereo Processing Engine

- Enabling generic obstacle detection, terrain modeling, and more

Advanced Image Processing

- Multi-exposure line-interleaved HDR
- Real time multi-scale / multi-FoV generation
- Hardware dewarping engine support
- Multiple camera support
- Superior low-light processing
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support

High-Efficiency Video Encoding

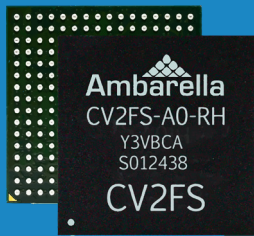
- 8MP30 H.264 video encoding performance
- Flexible multi-streaming capability
- Multiple constant bit rate (CBR) and variable bit rate (VBR) control modes
- Smart H.264 encoder algorithms

Functional Safety

- Error correcting code (ECC) protection of on-chip memory on DRAM
- Central error handling unit (CEHU)
- ISO 26262 compliant to meet ASIL C

Target Applications

- Single- / multi-camera advanced driver assistance systems (ADAS)
- Driver monitoring systems (DMS) and in-cabin solutions
- Single- / multi-channel electronic mirrors with blind spot detection (BSD)
- Parking assistance systems



The CV2FS chip targets automotive sensing camera designs.

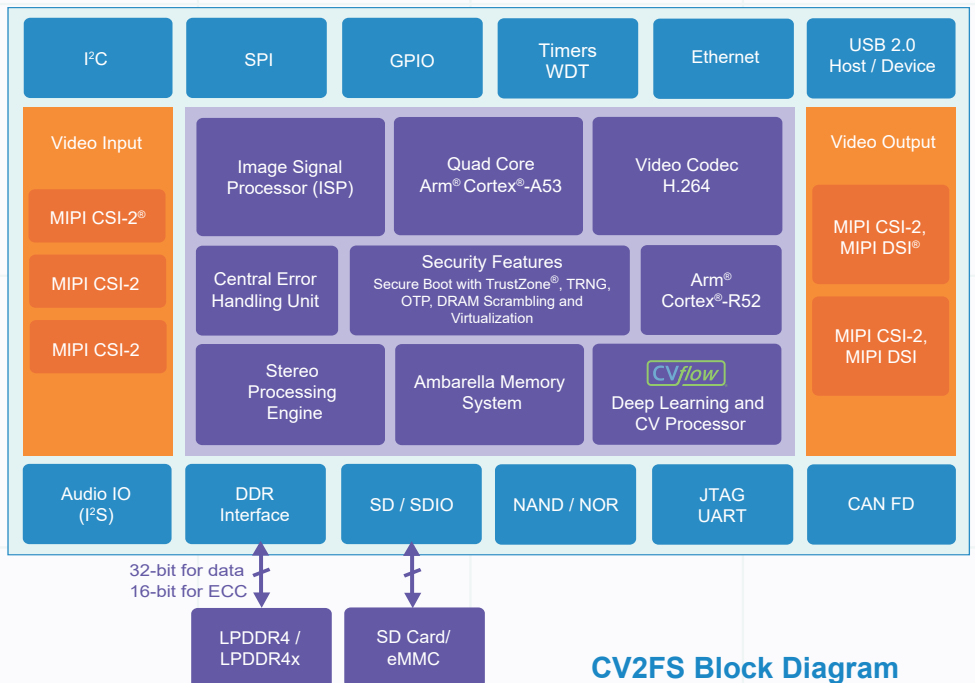


Overview

Ambarella's ASIL C-compliant CV2FS combines high-performance and power-efficient computer vision acceleration, superior image processing (ISP), and H.264 video compression in a single system on chip (SoC). Ambarella's highly efficient CVflow® computer vision engine delivers DNN processing and a dedicated stereo vision accelerator to enable efficient implementation of mono and stereo algorithms for the next generation of intelligent automotive cameras.

The ISP provides outstanding imaging in low-light conditions while its high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, enhancing the computer vision capabilities of the chip while delivering crisp video for driver viewing. CV2FS delivers high-resolution video recording and streaming at very low bit rates with efficient encoding in H.264 video format. It includes a suite of advanced cybersecurity features such as secure boot with TrustZone® and secure memory, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and virtualization, and a programmable secure level for each peripheral interface.

Fabricated in advanced 10 nm process technology, the CV2FS achieves an industry-leading combination of high performance and low power for computer vision applications. It is an ideal platform for implementing single- and multi-camera ADAS, DMS and in-cabin solutions, single- and multi-channel electronic mirrors with BSD, and intelligent parking assistance systems.



CV2FS Block Diagram

General Specifications

Processor Cores

- Quad-core Arm®Cortex®-A53 up to 1 GHz
 - 32 KB / 32 KB L1 cache, 1 MB L2 cache
- Arm Cortex-R52 456 MHz with dual-core lock step (DCLS)
 - 32 KB / 32 KB I/D L1 cache, 1 MB of embedded SRAMs
- NEON™ SIMD and FPU acceleration
- AES / SHA1 / SHA2-256 crypto acceleration using Arm V8 extensions

Computer Vision Processor

- CVflow processor optimized for high-performance CNN / DNN execution
- Disparity mapping
- Dense optical flow engine

Video Input

- Multi-sensor input with independent ISP configuration
- Three MIPI CSI-2® ports (one port with virtual channels)

Video Output

- Two MIPI CSI-2 / MIPI DSI® ports
- On-screen display (OSD) engine and overlays

CMOS Sensor / Image Processing

- Processing up to 480 MPixel/s
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)

- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Adjustable auto exposure (AE) / auto white balance (AWB)
- Dynamic range (WDR and HDR) engine
- Chromatic aberration correction
- Geometric distortion correction
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

Video Encoding

- H.264 MP / HP L5.0
- 8MP30 maximum encoding performance
- Flexible GOP configuration with I and P frames
- Multiple CBR and VBR rate control modules

Security Features

- Secure boot with TrustZone®, TRNG, OTP, DRAM scrambling and virtualization

Tools for Development

- CNN toolkit to ease the porting of CNNs trained using frameworks such as Caffe, TensorFlow, or ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

Memory Interfaces

- LPDDR4x / LPDDR4 up to 1.8 GHz clock rate, 32-bit data bus for data and 16-bit data bus for ECC, up to 4 GB capacity
- Two SD controllers
- Boot from SPI / SPI NAND with BCH / SPI NOR / USB / eMMC
- Single- / dual- / quad- / octal-SPI NOR and single- / dual- / quad-SPI NAND

Peripheral Interfaces

- Six CAN FD controllers
- Two Ethernet ports with data transfer rates of 10- / 100- / 1000-Mbps
- One USB 2.0 port configurable as device / host with PHY
- Multiple SSI / SPI, IDC, and UART
- Multiple GPIO ports, PWM, steppers, ADC
- Watchdog timer, general purpose timers, and JTAG
- Audio interface (I²S)

Physical

- 10 nm low power complimentary metal-oxide semiconductor (CMOS)
- FC TFBGA package (14x14 mm, 0.65 mm pitch)
- Operating temperature -40°C to +125°C (T_j)
- Automotive qualified (AEC-Q100 Grade-2, ASIL C)

CV2FS Camera Development Platform

The CV2FS camera development platform contains the necessary tools, software, hardware, and documentation to develop a camera utilizing the powerful CVflow processor while supporting development of customized features.

Evaluation Kit (EVK)

- CV2FS main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, onsemi, Omnivision, and others
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code available with additional licensing

Software Development Kit (SDK)

- ISO 26262-compliant SDK, OS, and middleware
- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Safety documentation for applications required to meet ISO 26262 standards
- Detailed documentation with programmer's guide and more
- CNN / DNN training, profiling, and porting tools

www.ambarella.com/contact-us/

Copyright Ambarella International LP. All rights reserved. Ambarella and the Ambarella logo are trademarks of Ambarella International LP. All other brands, product names, and company names are trademarks of their respective owners. The information in this document is believed to be reliable, but may project preliminary functionality not yet available. Ambarella makes no guarantee or warranty concerning the accuracy and availability of said information and shall not be responsible for any loss or damage whatever nature resulting from the use of, or reliance upon it. Ambarella does not guarantee that the use of any information contained herein will not infringe upon patent, trademark, copyright, or other rights of third parties. Ambarella reserves the right to make changes in the product and /or its specifications presented in this publication at any time without notice.