

# CV25S

Computer Vision SoC for IP Cameras

## Key Features

### Flexible Low-Power Platform

- CVflow<sup>®</sup> computer vision engine
- 64-bit quad-core Arm<sup>®</sup> Cortex<sup>®</sup>-A53 CPU up to 1 GHz
- Linux kernel version 4.14 or later (64-bit)
- Linux SDK for standards-based development
- Secure boot with TrustZone<sup>®</sup> and secure memory, TRNG, OTP, DRAM scrambling and virtualization
- Industry-leading image sensor support
- 10 nm low-power CMOS process

### CVflow Computer Vision Engine

- CNN / DNN inference acceleration for detection, classification, and more
- CNN toolkit for easy porting with Caffe, TensorFlow, and ONNX
- Tools for high- and low-level algorithm development

### Advanced Image Processing

- Up to 504 MPixel/s input rate
- Multi-exposure line-interleaved HDR
- Superior low-light processing
- 3D motion-compensated temporal filtering (MCTF)
- Hardware dewarping engine
- Electronic image stabilization (EIS)
- Up to three independent sensor inputs

### High-Efficiency Video Encoding

- H.265 and H.264 video compression
- Flexible multi-streaming capability
- 4KP30+ video performance
- Multiple CBR and VBR bit rate control modes
- Smart H.264 and H.265 encoder algorithms



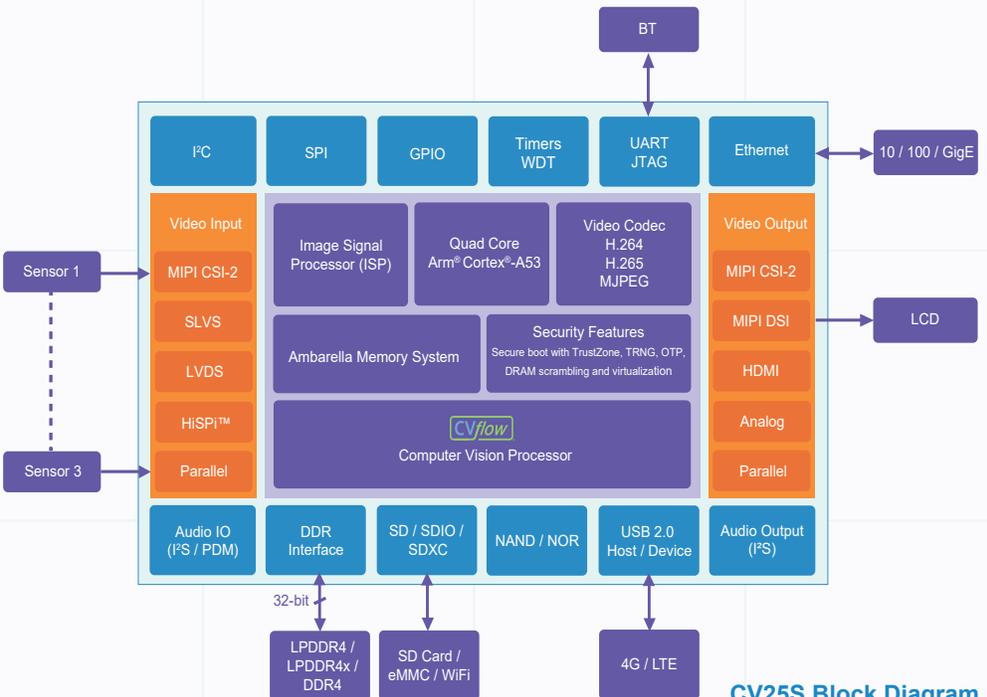
## Overview

Ambarella's CV25S SoC combines state-of-the-art computer vision technology with image processing in a single, low-power design. Fabricated using advanced 10 nm process technology, CV25S achieves an industry-leading combination of low power and high performance in both human and computer vision applications.

Meeting the demands of the next generation of intelligent IP cameras, CV25S's CVflow<sup>®</sup> architecture provides deep neural network (DNN) computer vision processing and 4KP30+ video encoding, enabling a multitude of computer vision applications on the edge. Efficiently encoding in both AVC and HEVC video formats, CV25S minimizes cloud storage costs by streaming high-resolution video at low bit rates.

To further enhance its computer vision capabilities, CV25S uses a next-generation image signal processor (ISP) to deliver outstanding imaging in low-light conditions, while its high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes.

CV25S includes a suite of advanced cybersecurity features such as secure boot with TrustZone<sup>®</sup> and secure memory, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and virtualization, and a programmable secure level for each peripheral interface. To help customers easily port their own neural networks onto the CV25S SoC, Ambarella's software development kit offers a complete set of tools.



CV25S Block Diagram

# General Specifications

## Processor Cores

- Quad-core Arm® Cortex®-A53 up to 1 GHz
- 32 KB / 32 KB I/D and 1 MB L2 cache
- NEON™ SIMD and FPU acceleration
- AES / SHA1 / SHA2-256 crypto acceleration
- Ambarella image signal processor and video codec

## Sensor and Video I/O

- Single, dual, or triple sensor input with independent ISP configuration
- Sub-LVDS / MIPI CSI-2 / SLVS / HiSPi™ input
- 16-bit parallel LVCMOS (BT.601 / 656)
- BT.601 / 656 16-bit video in and 16-bit BT.601 out
- HDMI® 2.0 including PHY with CEC support
- PAL / NTSC composite SD video
- 4-lane MIPI DSI / CSI-2 and FPD (VESA / JEIDA) out

## Sensor Processing

- 504 MPixel/s maximum pixel rate
- Lens shading correction
- Multi-exposure HDR (line-interleaved sensors)
- WDR with local tone mapping

## Image Processing

- 3D motion-compensated temporal filtering (MCTF)
- 3-axis electronic image stabilization (EIS)
- Adjustable AE / AWB / AF
- 180° and 360° fisheye lens distortion correction

- High quality polyphase scalars
- Digital PTZ and virtual cameras
- OSD engine, overlays, and privacy mask
- Crop, mirror, flip, 90° / 270° rotation
- DC-iris and P-iris
- Defective pixel correction
- Geometric lens distortion correction
- Chromatic aberration correction
- Gamma compensation and color enhancement
- Backlight compensation

## Intelligent Video Analytics

- CVflow® vision processor for CNN / DNN edge analytics
- People counting and tracking
- Face detection and recognition
- Human / pet / vehicle classification
- Object classification, recognition, and more
- License plate recognition

## Video Encoding

- H.265 MP L5.1, H.264 MP / HP L5.1, and MJPEG
- 4KP30+ maximum encoding performance
- Up to 8 simultaneous stream encodes
- Flexible GOP configuration with I, P, and B frames
- Temporal scalable video codec (SVC-T) with 4 layers
- Dynamic region of interest (ROI)
- Multiple CBR and VBR rate control modules

## Security Features

- Secure boot with TrustZone® and secure memory, TRNG, OTP, DRAM scrambling and virtualization

## Memory Interfaces

- LPDDR4 / LPDDR4x / DDR4 up to 1.6 GHz, 32-bit data bus
- Three SD controllers: SD / SDIO / SDXC
- Boot from SPI or parallel SLC NAND with BCH / SPI NOR / USB / eMMC

## Peripheral Interfaces

- 10 / 100 / 1000 Ethernet with RMII / RGMII
- One USB 2.0 port configurable as host / device
- Audio interface including I2S and DMIC
- Multiple SSI / SPI, I2C, and UART
- Multiple GPIO ports, PWM, IR, and ADC
- Watchdog timer, multiple general purpose timers, and JTAG

## Physical

- 10 nm low-power CMOS
- Operating temperature -25°C to +85°C
- FC TFBGA package (361 balls, 13x13 mm, 0.65 mm pitch)

## CV25S Camera Development Platform

The CV25S camera development platform contains the necessary tools, software, hardware, and documentation to develop a camera utilizing the powerful CVflow processor while supporting the development of customized features.

### Evaluation Kit

- CV25S main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, ON Semi, Omnivision, and others
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code

### Software Development Kit

- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation, including a programmer's guide and more
- CNN / DNN model preparation, porting, and profiling tools

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