

CV25AQ

Automotive Computer Vision SoC

Key Features

Computer Vision Engine CVflow®

- CNN- / DNN-based processing to enable detection, classification, tracking, and more
- Tools for high- and low-level algorithm development
- CNN toolkit for easy porting with Caffe, TensorFlow, and ONNX

Advanced Image Processing

- Multi-exposure line-interleaved HDR
- Hardware dewarping engine support
- Electronic image stabilization (EIS)
- Multiple camera support
- Advanced LED flicker mitigation
- 3D motion compensated temporal filtering (MCTF)
- Superior low-light processing
- RGGG / RCCB / RCCC / RGB-IR / monochrome sensor support

High-Efficiency Video Encoding

- H.265 and H.264 video compression
- Flexible multi-streaming capability
- 6MP30 video performance
- Multiple CBR and VBR control modes
- Smart H.264 and H.265 encoder algorithms

Target Applications

- Multi-channel drive recorders
- Single- / dual-channel electronic mirrors
- Driver / in-cabin monitoring systems (DMS / CMS)

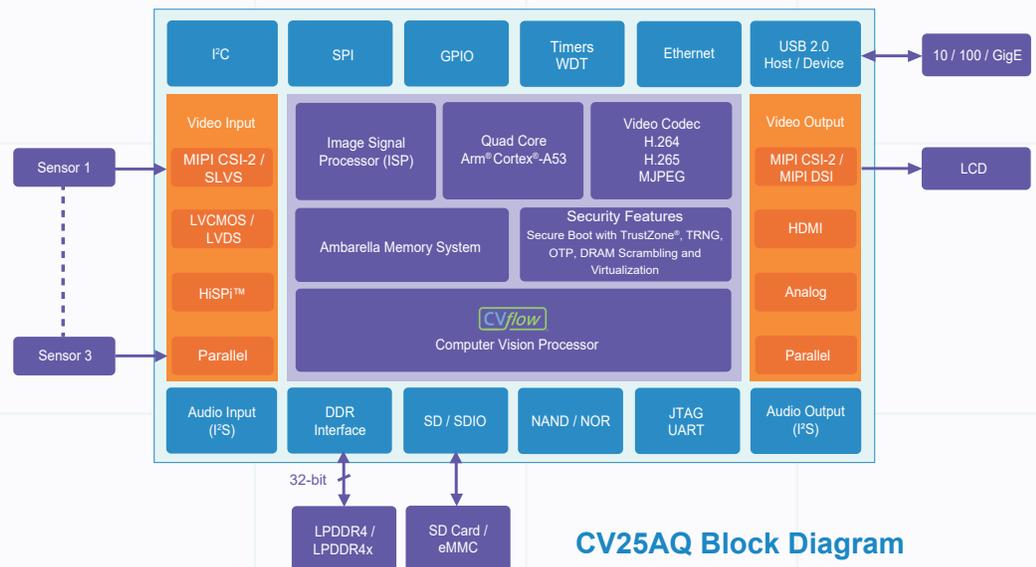


Overview

Ambarella's AEC-Q100 qualified CV25AQ SoC combines image processing, 6MP30 video encoding / decoding, and CVflow® computer vision processing in a single, low-power design. The CV25AQ's CVflow architecture provides the deep neural network (DNN) required by the next generation of intelligent automotive cameras. Fabricated in advanced 10 nm process technology, CV25AQ achieves an industry-leading combination of low power and high performance in both human vision and computer vision applications. It is an ideal platform for implementing multi-channel digital video recorders, single- or dual-channel electronic mirrors with recording capabilities, driver / in-cabin monitoring cameras, and more.

The CV25AQ's CVflow architecture provides computer vision processing at 6MP resolution, enabling image recognition over long distances and with high accuracy. It includes efficient encoding in both AVC and HEVC video formats, delivering high-resolution video encoding with very low bit rates. The CV25AQ's next-generation image signal processor (ISP) provides outstanding imaging in low-light conditions, while its high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, further enhancing the computer vision capabilities of the chip.

CV25AQ includes a suite of advanced cyber-security features such as secure boot with TrustZone® and secure memory, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and virtualization, and a programmable secure level for each peripheral interface. To help customers easily port their own neural networks onto the CV25AQ SoC, Ambarella's software development kit offers a complete set of tools.



CV25AQ Block Diagram

General Specifications

Processor Cores

- Quad-core Arm® Cortex®-A53 up to 756 MHz
- 32 KB / 32 KB I/D and 1 MB L2 cache
- NEON™ SIMD and FPU acceleration
- AES / SHA1 / SHA2-256 crypto acceleration

Video Input

- Single, dual, or triple sensor inputs with independent ISP configuration
- LVDS / MIPI CSI-2 / SLVS / HiSPi™
- 16-bit parallel LVCMOS (BT. 601 / 656)

Video Output

- 16-bit parallel LVCMOS (BT. 601)
- HDMI® 2.0 including PHY with CEC support
- PAL / NTSC composite SD video
- MIPI DSI / CSI-2 and FPD (VESA / JEIDA) out

CMOS Sensor / Image Processing

- 6MP30 maximum input resolution
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)
- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Adjustable AE / AWB
- LED flicker compensation for LED sources
- High dynamic range (HDR) engine
- Chromatic aberration correction
- 180° fisheye lens and geometric distortion correction
- OSD engine and overlays
- Gamma compensation and color enhancement

- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

Video Encoding / Decoding

- H.265 (HEVC) MP L5.1, H.264 MP / HP L5.1, and MJPEG
- 6MP30 maximum encoding / decoding performance
- Flexible GOP configuration with I, P, and B frames
- Multiple CBR and VBR control modules

Computer Vision Processor

- CVflow processor with parallel architecture to boost performance of the low-level portion of perception algorithms

Tools for Development

- CNN toolkit to ease the porting of CNN trained with Caffe, TensorFlow, or ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

Security Features

- Secure boot with TrustZone® and secure memory, TRNG, OTP, DRAM scrambling and virtualization

Memory Interfaces

- LPDDR4x / LPDDR4 up to 1.2 GHz clock rate, 32-bit data bus, up to 2 GB capacity
- Three SD controllers
- Boot from SPI / parallel SLC NAND with BCH / SPI NOR / USB / eMMC
- Single- / dual- / quad-SPI NOR and SPI NAND

Peripheral Interfaces

- 10 / 100 / 1000 Ethernet AVB with RMII / RGMII
- One USB 2.0 port configurable as device / host with PHY
- Audio interface including I²S and DMIC
- Multiple SSI / SPI, IDC, and UART
- Multiple GPIO ports, PWM, steppers, IR, and ADC
- Watchdog timer, multiple general purpose timers, and JTAG

Physical

- 10 nm low-power CMOS
- FC TFBGA package (361 balls, 13x13 mm, 0.65 mm pitch)
- Operating temperature -40°C to + 105°C
- Automotive qualified (AEC-Q100 Grade-2)

CV25AQ Camera Development Platform

The CV25AQ camera development platform contains the necessary tools, software, hardware, and documentation to develop a camera utilizing the powerful CVflow processor while supporting development of customized features.

Evaluation Kit

- CV25AQ main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, ON Semi, Omnivision, and others
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code

Software Development Kit

- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation, including a programmer's guide and more
- CNN / DNN training, profiling, and porting tools

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