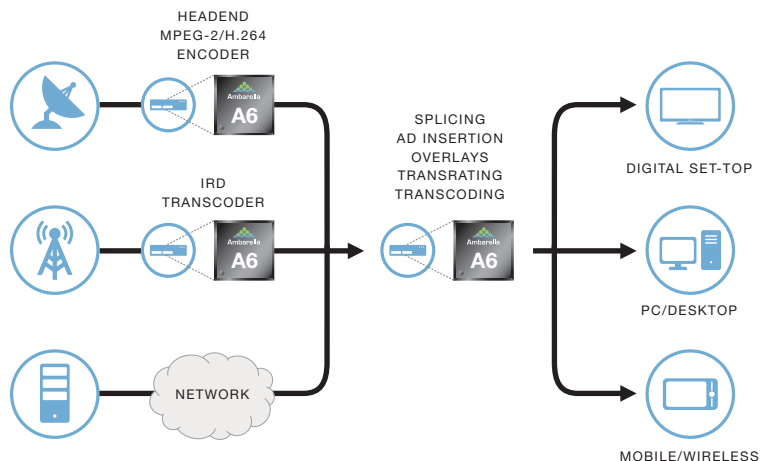




A6 Broadcast Encoder/Transcoder

Overview

The A6 is an encoder/transcoder chip for H.264 and MPEG-2 broadcast distribution applications, delivering an unmatched combination of picture quality and stream density. A single A6 is capable of 1080p60 encoding with RDO and full HD transcoding using decode and encode for optimum coding efficiency. The platform supports development of fully-featured high-density transcoders and multi-pass headend encoders, while offering functions such as splicing, rateshaping and adaptive streaming for the Adobe/Apple/Microsoft formats.



A wide spectrum of high-performance applications is supported by A6.

Key Features

Single Platform, Many Uses

- HD/SD encode, decode and transcode
- Overlays, splicing, rate shaping, ad insertion

Promotes Differentiation

- Easy-to-use high-level ARM APIs and SDK
- Flexible DSP video engine

High Efficiency and High Density

- Low-power CMOS design
- Compact 32-bit DDR design

High Performance Video Engine

- 3D MCTF noise reduction
- 1080p60 or 4xSD+PIPs H.264 encode

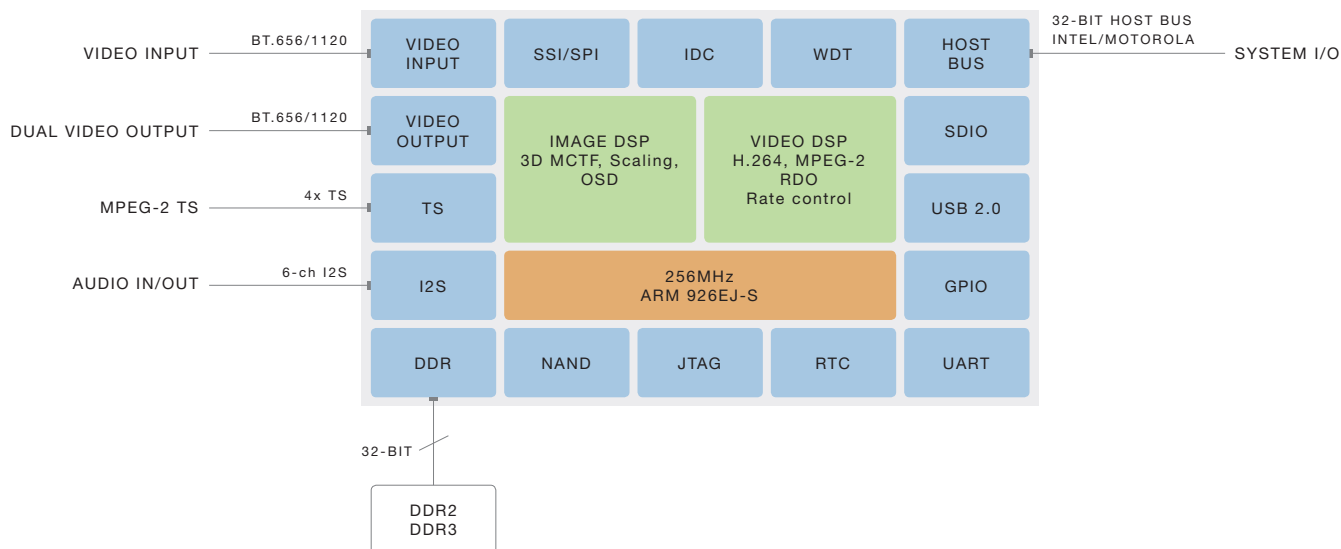
Superior Quality HD Encoding

- Ambarella's industry-leading H.264 codec
- Single-chip, or multi-chip multi-pass systems

High-Quality MPEG-2 ↔ H.264 Transcoding

- Full decode to encode with metadata
- Multi-resolution, multi-rate, multi-profile

Block Diagram





A6 Broadcast Encoder/Transcoder

General Specifications

Video Input/Output

- CCIR.601/656 in (up to 148.5MHz)
- Two ITU-R BT.601/656 out (16/24-bit YUV)
- Four MPEG-2 TS (4-wire serial and 8-bit parallel)

Video CODECs

- H.264 BP/MP/HP up to Level 4.1
- MPEG-2 MP@ML/HL
- 1920x1080p60 H.264/MPEG-2 encode/decode
- Full decode-encode transcoding
 - 1920x1080i60 H.264 ↔ MPEG-2 transcode
 - Dual 1080i60 MPEG-2 to SD transcode
 - HD/SD to multi-stream progressive transcode
 - Multi-resolution, multi-rate, multi-profile
 - PTS preservation throughout system
 - Discontinuity and meta data handling
- Wide range of coding modes
 - Low delay and high compression
 - High-precision ME and MD
 - Hierarchical B, Rate-Distortion Optimization, Multiple Ref Frames, Adaptive QP, etc.
- Other
 - Scene detection
 - Telecine handling
 - F-code assessment
 - Advanced CBR/VBR rate control

Image Processing

- 3D MCTF noise reduction, color space conversion, alpha-blending OSD, picture statistics, scaling

Audio

- AAC/AC-3 decode/encode
- AC-3 5.1 encode, MP3 decode

CPU

- ARM926EJ-S + Ambarella multi-core DSP engine
- AES/DES/3DES cryptographic acceleration

Peripherals

- 32-bit DDR2 or DDR3
- 32-bit Host i/f (Intel/Motorola style)
- 2x I2S ports (6-ch)
- HDMI 1.2
- USB 2.0 Device
- NAND/EEPROM
- SSI/SPI, I2C, GPIO, UART, JTAG, SDIO, RTC, WDT

Physical

- Power typical 2.5 Watts incl. DDR3
- 596-ball PBGA, 21x21mm

A6 Broadcast Development Platform

The A6 Broadcast Development Platform contains the necessary tools, software, hardware and documentation to evaluate and perform software development.

Hardware Platform

- A6 main board
- Video input and ASI input/output card
- JTAG adapter

Software Development Kit (SDK)

- eSol RTOS and tool chain
- Encoder/transcoder demo application with ARM source

Documentation

- Programmer's guide, application notes
- A6 datasheet, BOM, schematics and layout



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